CMOS image sensor architecture for high-speed sparse image content readout

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Requirements and applications

Many high-end imaging systems such as used in particle detection [1] or the High Atmosphere Lightning Study [2], make use of high-speed image sensor. These imagers operate with readout times in the range of 100µs to 1ms. They have resolutions in the Megapixel range and produce several thousands of frames per second.

Fully synchronous high-speed image sensor are notably inefficient in terms of power. They consume several Watts and are complex to use and interface due to the large amount of high bandwidth parallel analog busses. However, in various cases where high-speed image sensors are required, it appears that the scene contains sparse and fugitive information.

To address this issue, we propose an architecture for image sensor readout using a pipelined global shutter image sensor in which the readout is asynchronous and not scanned sequentially. Content aware pixels use a domino-like asynchronous readout and do not suffer from ambiguity during the decoding of the addresses. The analog data are then retrieved from the single pixels using the asynchronously read addresses.

Principle

As in retina-like image sensors [3], some of the image processing is done within the pixel [4, 6-11] (Fig. 1). We added a decision circuit to the shutter of each pixel to produce a logic flag. This flag is used to retrieve the address (position) of the pixel as shown in Fig. 2.

The shift register propagates a logical “token” along the columns of pixels, activating the columns one after an other. When a pixel of the current activated column has its decision circuit flag set, its switch is closed and a logical “1” is present on the corresponding row input of the asynchronous scan. The asynchronous scan scans all the rows and the ones containing a “1” have their corresponding row generated and sent to the controller. Once all the addresses of the active rows have been read then the shift register shifts the “1” token to the next column.

As this is digitally scanned, even for the worst case scan time, i.e. all pixels flagged, is a few 100µs for a 512x512 pixel array. Afterwards, analog readout may take place of those pixels that have been identified as interesting. The shift register requires 10nJ/column with our chip while the asynchronous reading of flagged rows needs about 30nJ/row (Fig 3).

References: